DIGITAL AUDIO

Digital Equalizer

YM3608 DEQ

■ OUTLINE

The YM3608 is a s pecial digital processor developed by Yamaha Corp. for use with digital filters. This processor makes it possible to easily configure IIR and FIR filters for serial sound signals using the internal microprogram.

This processor also makes possible high accuracy calculations and the freedom to rewrite microprogram functions and coefficients using SCI*.

* SCI: Serial Control Interface (refer to II-2-1)

■ FEATURES

1. **All microprogramable function for digital filter.**
2. **Multiplication is performed with one clock for Data 16 bits × Coefficient 32 bits. (2 clocks for Data 32 bits × Coefficient 32 bits) (This is 5-clock pipeline processing.)**
3. **There are 2 serial input terminals and 2 serial output terminals, both of which can be used with any desired timing. The MSB/LSB first and shift clocks can be selected independently for input and output. Input and output are also possible using an external clock.**
4. **A 50-bit accumulator with 4 bits of head margin and overflow detect is provided.**
5. **The master clock operates at a maximum phase of 4.4MHz and a minimum phase of 2MHz.**
6. **Microprogram and coefficients can be controlled with SCI (Serial Control Interface).**
7. **Up to 128 steps can be used with microprogram.**
8. **Higher calculation performance is possible by making a serial connection to YM3608 (DEQ).**
9. **Operates on a single 5V power supply.**
10. **24-pin DIP.**

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Rating
Power supply voltage	V_{DD}	−0.3 ~ 7.0V
Input voltage	V_I	−0.3 ~ V_{DD} + 0.5V
Operating temperature	T_{OP}	0 ~ 70°C
Storage temperature	T_{stg}	−50 ~ 125°C

Recommended Operating Conditions

Item	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0		70	°C

D.C. Characteristics

Item	Symbol	Minimum	Typical	Maximum	Unit
Input clock frequency	fc	2		4.4	MHZ
Input clock High level time	$T_{\Phi H}$	90			n sec
Input clock Low level time	$T_{\Phi L}$	100			n sec
Input data set-up time	T_{DS}	50			n sec
Input data hold time	T_{DH}	10			n sec
Output delay time *1	T_{OD}			100	n sec
Bypass delay time *1	$T_{\beta D}$			70	n sec

Conditions: V_{DD} = 5.0V ± 5%, T_{OP} = 0 ~ 70°C

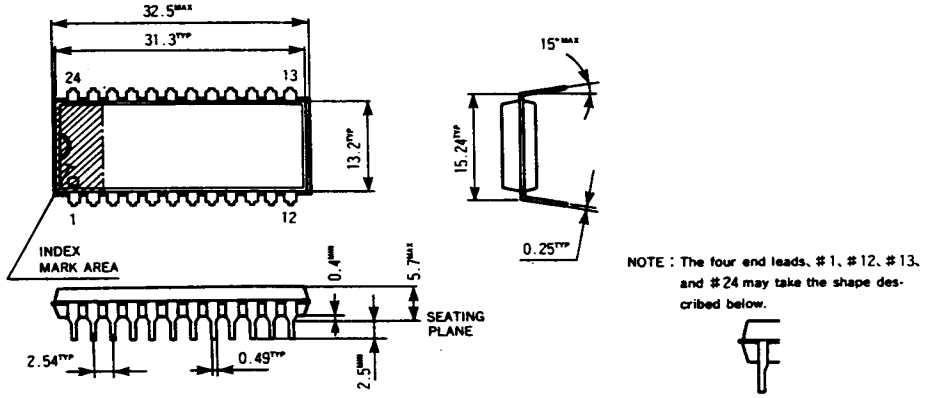
A.C. Characteristics

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Output voltage H level	V_{OH}	I_{OH} = −0.4mA	3.5		V_{DD}	V
Output voltage L level	V_{OL}	I_{OL} = 1mA	V_{SS}		0.4	V
Input voltage H level	V_{IH}		2.4			V
Input voltage L level	V_{IL}				0.4	V
Input leak current	I_{LK}	V_I = 5V			0.1	μA

*1: with 100pF capacitance added.

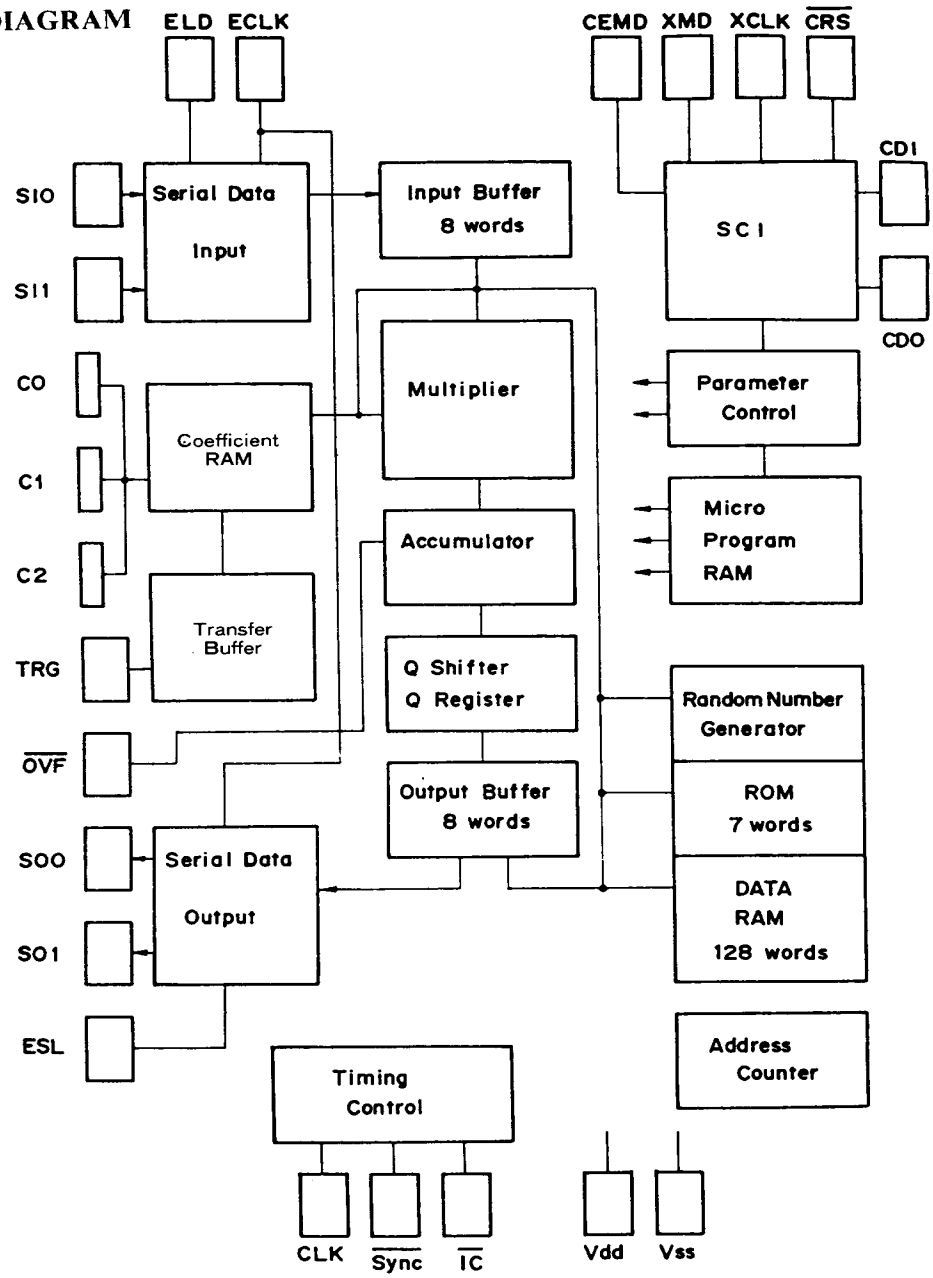
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■ OUTLINE DIMENSIONS



NOTE : The four end leads, #1, #12, #13, and #24 may take the shape described below.

■ BLOCK DIAGRAM



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